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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/714,801	11/17/2003	Yun-Ho Choi	SAM-0486	2965
7590		11/08/2005	EXAMINER	
Steven M. Mills		GRAYBILL, DAVID E		
MILLS & ONELLE LLP		ART UNIT		
Suite 605		PAPER NUMBER		
Eleven Beacon Street		2822		
Boston, MA 02108		DATE MAILED: 11/08/2005		

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/714,801

Applicant(s)

CHOI ET AL.

Examiner

David E. Graybill

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 August 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) 13 and 14 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-12 and 15-18 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 17 November 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 1 page.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

Claims 13 and 14 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 8-31-5.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the feature, "solder bump," of claims 6, 10 and 16 must be shown or the feature canceled from the claims.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet"

pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-12 and 15-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 1-12 and 15-18 the scope of the term "type" cannot be determined because the common qualities that distinguish the individual members of the class *type* as an identifiable class are not recited in the claims, and they cannot otherwise be determined.

There is insufficient antecedent basis for the following language:

Claims 5, 7, 9, 11, 12, 15 and 17, "the package type";

Claims 8 and 18, "their back surfaces."

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for

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patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 1 is rejected under 35 U.S.C. 102(e) as being clearly anticipated by Corisis (6607937).

At column 4, line 45 to column 5, line 25; and column 5, line 60 to column 6, line 37 Corisis discloses

A stack type multi-chip package comprising: a first semiconductor chip 424a which shows good results when tested for reliability after being assembled at a package level; at least one second semiconductor chip 424b which is in a wafer level configuration and is stacked on the first semiconductor chip via stacking means "adhesive"; a first connecting unit 443a for electrically connecting the first semiconductor chip to an external system 430; and a second connecting unit 443b for electrically connecting the second semiconductor chip to the external system, wherein the first connecting unit is different from the second connecting unit.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 2-4, 9 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Corisis as applied to claim 1, and further in combination with Bolkin (6798057).

As cited, Corisis discloses a printed circuit board 430 for the multi-chip package, which includes bonding pads 431a to which the first connecting unit and the second connecting unit are connected; a molding compound 423c for fastening the first and second semiconductor chips and protecting the first and second semiconductor chips from the external environment; wherein the stacking means are an adhesive; wherein the package type of the first semiconductor chip is a BGA.

However, Corisis does not appear to explicitly disclose pins for connecting the bonding pads to the external system.

Nonetheless, at column 4, line 63 to column 5, line 12, Bolkin discloses "TQFP's" and TQFP's inherently have pins for connecting to external systems. Moreover, it would have been obvious to combine this disclosure of Bolkin with the disclosure of Corisis because it would provide electrical connectivity of the printed circuit board bonding pads to external power sources and components.

Also, Corisis does not appear to explicitly disclose; wherein the package type of the first semiconductor chip is a Thin Quad Flat package (TQFP) or a Super Thin Small Outline Package (STSOP).

Still, as cited, Corisis discloses that the package type of the first semiconductor chip is a ball grid array. Furthermore, as cited, Bolkin discloses that a ball grid array and a TQFP are alternatives and equivalents; therefore, it would have been obvious to substitute the TQFP of Bolkin for the ball grid array of Corisis. See *In re May* (CCPA) 136 USPQ 208 (It is our opinion that the substitution of Wille's type seal for the cement of Hallauer in Figure 1 would be obvious to persons of ordinary skill in the art from the disclosures of these references, merely involving an obvious selection between known alternatives in the art and the application of routine technical skills.); *In re Cornish* (CCPA) 125 USPQ 413; *In re Soucy* (CCPA) 153 USPQ 816; *Sabel et al. v. The Wickes Corporation et al.* (DC SC) 175 USPQ 3; *Ex parte Seiko Koko Kabushiki Kaisha Co.* (BdPatApp&Int) 225

USPQ 1260; and Ex parte Rachlin (BdPatApp&Int) 151 USPQ 56. See also Smith v. Hayashi, 209 USPQ 754 (Bd. of Pat. Inter. 1980) (However, there was evidence that both phthalocyanine and selenium were known photoconductors in the art of electrophotography. "This, in our view, presents strong evidence of obviousness in substituting one for the other in an electrophotographic environment as a photoconductor." 209 USPQ at 759.). An express suggestion to substitute one equivalent component or process for another is not necessary to render such substitution obvious. In re Fout, 675 F.2d 297, 213 USPQ 532 (CCPA 1982). "It is prima facie obvious to combine two compositions each of which is taught by the prior art to be useful for the same purpose, in order to form a third composition to be used for the very same purpose.... [T]he idea of combining them flows logically from their having been individually taught in the prior art." In re Kerkhoven, 626 F.2d 846, 850, 205 USPQ 1069, 1072 (CCPA 1980) (citations omitted). See also In re Crockett, 279 F.2d 274, 126 USPQ 186 (CCPA 1960); Ex parte Quadranti, 25 USPQ2d 1071 (Bd. Pat. App. & Inter. 1992).

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Corisis and Bolkin as applied to claim 4, and further in combination with Koh (6737738).

Corisis and Bolkin do not appear to explicitly disclose wherein the package type of the first semiconductor chip is a Fine Ball Grid Array (FBGA) or a Wafer-Level Chip Size Package (W-CSP).

Nevertheless, as cited, Corisis discloses that the package type of the first semiconductor chip is a ball grid array. Further, at column 4, lines 13-23, Koh discloses wherein the package type of the first semiconductor chip 22 is a Fine Ball Grid Array (FBGA). Therefore, it would have been obvious to combine this disclosure with the disclosure of Corisis because it would facilitate provision of the ball grid array of Corisis.

Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Corisis, Bolkin and Koh as applied to claim 5, and further in combination with Yanagida (20010042923) and Jiang (6906415).

Corisis, Bolkin and Koh do not appear to explicitly disclose wherein the first connecting unit is a solder bump for connecting solder balls of the FBGA or the W-CSP to the bonding pads of the printed circuit board.

Regardless, at paragraph 127, Yanagida discloses wherein the first connecting unit is a solder bump 119 for connecting solder balls 116b of a BGA 110 to the bonding pads 211 of the printed circuit board 210. In addition, it would have been obvious to combine this disclosure of Yanagida with the disclosure of Corisis, Bolkin and Koh because it would facilitate electrical connection.

Also, Corisis, Bolkin, Koh and Yanagida do not appear to explicitly disclose that the second connecting unit is bonding wires for connecting pads of the second semiconductor chip to the bonding pads of the printed circuit board.

Notwithstanding, as cited, Corisis discloses that the second connecting unit is "pins." Furthermore, in claim 53, Jiang discloses that pins and bonding wires are alternatives and equivalents; therefore, it would have been obvious to substitute the bonding wires of Jiang for the pins of Corisis. See *In re May* (CCPA) 136 USPQ 208 (It is our opinion that the substitution of Wille's type seal for the cement of Hallauer in Figure 1 would be obvious to persons of ordinary skill in the art from the disclosures of these references, merely involving an obvious selection between known alternatives in the art and the application of routine technical skills.); *In re Cornish* (CCPA) 125 USPQ 413; *In re Soucy* (CCPA) 153 USPQ 816; *Sabel et al. v. The Wickes Corporation et al.* (DC SC) 175 USPQ 3; *Ex parte Seiko Koko Kabushiki Kaisha Co.* (BdPatApp&Int) 225 USPQ 1260; and *Ex parte Rachlin* (BdPatApp&Int) 151 USPQ 56. See also *Smith v. Hayashi*, 209 USPQ 754 (Bd. of Pat. Inter. 1980) (However, there was evidence that both phthalocyanine and selenium were known photoconductors in the art of electrophotography. "This, in our view, presents strong evidence of obviousness in substituting one for the other in an electrophotographic

environment as a photoconductor." 209 USPQ at 759.). An express suggestion to substitute one equivalent component or process for another is not necessary to render such substitution obvious. In re Fout, 675 F.2d 297, 213 USPQ 532 (CCPA 1982). "It is prima facie obvious to combine two compositions each of which is taught by the prior art to be useful for the same purpose, in order to form a third composition to be used for the very same purpose.... [T]he idea of combining them flows logically from their having been individually taught in the prior art." In re Kerkhoven, 626 F.2d 846, 850, 205 USPQ 1069, 1072 (CCPA 1980) (citations omitted). See also In re Crockett, 279 F.2d 274, 126 USPQ 186 (CCPA 1960); Ex parte Quadranti, 25 USPQ2d 1071 (Bd. Pat. App. & Inter. 1992).

Corisis, Koh, Yanagida and Jiang also do not appear to explicitly disclose wherein the package type of the printed circuit board is a Ball Grid Array (BGA).

Still, as cited, Bolkin discloses wherein the package type of the printed circuit board 202 is a Ball Grid Array (BGA). In addition, it would have been obvious to combine this disclosure of Bolkin with the disclosure of the applied prior art because it would provide electrical connectivity of the printed circuit board of the applied prior art to any external power sources and components.

Also, in the combination of applied prior art, Corisis discloses wherein the first semiconductor chip and the second semiconductor chip are stacked via the adhesive such that their back surfaces face each other.

Claims 10-12 and 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Corisis and Bolkin as applied to claims 9 and 15, and further in combination with Yanagida (20010042923) and Jiang (6906415).

Corisis and Bolkin do not appear to explicitly disclose wherein the first connecting unit is a solder bump for connecting pins of the TQFP or the STSOP to the bonding pads of the printed circuit board.

Nonetheless, at column 2, line 50 to column 3, line 6, Nguyen discloses wherein the first connecting unit is a solder bump for connecting pins of the TQFP 110 to the bonding pads 222 of the printed circuit board 210. Moreover, it would have been obvious to combine this disclosure of Nguyen with the disclosure of Corisis and Bolkin because it would facilitate electrical connection.

Also, Corisis and Bolkin do not appear to explicitly disclose that the second connecting unit is bonding wires for connecting pads of the second semiconductor chip to the bonding pads of the printed circuit board.

Notwithstanding, as cited, Corisis discloses that the second connecting unit is "pins." Furthermore, in claim 53, Jiang discloses that pins and bonding wires are alternatives and equivalents; therefore, it would have

been obvious to substitute the bonding wires of Jiang for the pins of Corisis. See *In re May* (CCPA) 136 USPQ 208 (It is our opinion that the substitution of Wille's type seal for the cement of Hallauer in Figure 1 would be obvious to persons of ordinary skill in the art from the disclosures of these references, merely involving an obvious selection between known alternatives in the art and the application of routine technical skills.); *In re Cornish* (CCPA) 125 USPQ 413; *In re Soucy* (CCPA) 153 USPQ 816; *Sabel et al. v. The Wickes Corporation et al.* (DC SC) 175 USPQ 3; *Ex parte Seiko Koko Kabushiki Kaisha Co.* (BdPatApp&Int) 225 USPQ 1260; and *Ex parte Rachlin* (BdPatApp&Int) 151 USPQ 56. See also *Smith v. Hayashi*, 209 USPQ 754 (Bd. of Pat. Inter. 1980) (However, there was evidence that both phthalocyanine and selenium were known photoconductors in the art of electrophotography. "This, in our view, presents strong evidence of obviousness in substituting one for the other in an electrophotographic environment as a photoconductor." 209 USPQ at 759.). An express suggestion to substitute one equivalent component or process for another is not necessary to render such substitution obvious. *In re Fout*, 675 F.2d 297, 213 USPQ 532 (CCPA 1982). "It is prima facie obvious to combine two compositions each of which is taught by the prior art to be useful for the same purpose, in order to form a third composition to be used for the very same purpose.... [T]he idea of combining them flows logically from their

having been individually taught in the prior art." In re Kerkhoven, 626 F.2d 846, 850, 205 USPQ 1069, 1072 (CCPA 1980) (citations omitted). See also In re Crockett, 279 F.2d 274, 126 USPQ 186 (CCPA 1960); Ex parte Quadranti, 25 USPQ2d 1071 (Bd. Pat. App. & Inter. 1992).

Corisis, Yanagida and Jiang also do not appear to explicitly disclose wherein the package type of the printed circuit board is a BGA.

Still, as cited, Bolkin discloses wherein the package type of the printed circuit board 202 is a Ball Grid Array (BGA). In addition, it would have been obvious to combine this disclosure of Bolkin with the disclosure of the applied prior art because it would provide electrical connectivity of the printed circuit board of the applied prior art to any external power sources and components.

Additionally, Corisis, Yanagida and Jiang do not appear to explicitly disclose wherein the package type of the printed circuit board is a TQFP.

Still, as cited, Bolkin discloses wherein the package type of the printed circuit board 202 is a TQFP. In addition, it would have been obvious to combine this disclosure of Bolkin with the disclosure of the applied prior art because it would provide electrical connectivity of the printed circuit board of the applied prior art to any external power sources and components.

Also, Corisis and Bolkin do not appear to explicitly disclose wherein the first connecting unit is a solder bump for connecting solder balls of the BGA to the bonding pads of the printed circuit board.

Regardless, at paragraph 127, Yanagida discloses wherein the first connecting unit is a solder bump 119 for connecting solder balls 116b of a BGA 110 to the bonding pads 211 of the printed circuit board 210. In addition, it would have been obvious to combine this disclosure of Yanagida with the disclosure of Corisis, Bolkin and Koh because it would facilitate electrical connection.

Corisis and Bolkin also do not appear to explicitly disclose that the second connecting unit is bonding wires for connecting pads of the second semiconductor chip to the bonding pads of the printed circuit board.

Notwithstanding, as cited, Corisis discloses that the second connecting unit is "pins." Furthermore, in claim 53, Jiang discloses that pins and bonding wires are alternatives and equivalents; therefore, it would have been obvious to substitute the bonding wires of Jiang for the pins of Corisis. See *In re May* (CCPA) 136 USPQ 208 (It is our opinion that the substitution of Wille's type seal for the cement of Hallauer in Figure 1 would be obvious to persons of ordinary skill in the art from the disclosures of these references, merely involving an obvious selection between known alternatives in the art and the application of routine technical skills.); *In re*

Cornish (CCPA) 125 USPQ 413; In re Soucy (CCPA) 153 USPQ 816; Sabel et al. v. The Wickes Corporation et al. (DC SC) 175 USPQ 3; Ex parte Seiko Koko Kabushiki Kaisha Co. (BdPatApp&Int) 225 USPQ 1260; and Ex parte Rachlin (BdPatApp&Int) 151 USPQ 56. See also Smith v. Hayashi, 209 USPQ 754 (Bd. of Pat. Inter. 1980) (However, there was evidence that both phthalocyanine and selenium were known photoconductors in the art of electrophotography. "This, in our view, presents strong evidence of obviousness in substituting one for the other in an electrophotographic environment as a photoconductor." 209 USPQ at 759.). An express suggestion to substitute one equivalent component or process for another is not necessary to render such substitution obvious. In re Fout, 675 F.2d 297, 213 USPQ 532 (CCPA 1982). "It is prima facie obvious to combine two compositions each of which is taught by the prior art to be useful for the same purpose, in order to form a third composition to be used for the very same purpose.... [T]he idea of combining them flows logically from their having been individually taught in the prior art." In re Kerkhoven, 626 F.2d 846, 850, 205 USPQ 1069, 1072 (CCPA 1980) (citations omitted). See also In re Crockett, 279 F.2d 274, 126 USPQ 186 (CCPA 1960); Ex parte Quadranti, 25 USPQ2d 1071 (Bd. Pat. App. & Inter. 1992).

Additionally, Corisis, Yanagida and Jiang do not appear to explicitly disclose wherein the package type of the printed circuit board is a TQFP.

Still, as cited, Bolkin discloses wherein the package type of the printed circuit board 202 is a TQFP. In addition, it would have been obvious to combine this disclosure of Bolkin with the disclosure of the applied prior art because it would provide electrical connectivity of the printed circuit board of the applied prior art to any external power sources and components.

Also, in the combination of applied prior art, Corisis discloses wherein the first semiconductor chip and the second semiconductor chip are stacked via the adhesive such that their back surfaces face each other.

The art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It is cited primarily to show inventions relevant to the examination of the instant invention.

For information on the status of this application applicant should check PAIR:

Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

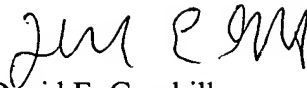
Alternatively, applicant may contact the File Information Unit at (703) 308-2733. Telephone status inquiries should not be directed to the examiner. See MPEP 1730VIC, MPEP 203.08 and MPEP 102.

Any other telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.
The fax phone number for group 2800 is (571) 273-8300.

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A handwritten signature in black ink, appearing to read "David E. Graybill".

David E. Graybill
Primary Examiner
Art Unit 2822

D.G.

3-Nov-05